Notice of Allowability	Application No.	Applicant(s)	
	09/560,364	LO ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed November 23, 2004*.

2. ☒ The allowed claim(s) is/are *claims 16-44 renumbered respectively as claims 1-28*.

3. ☒ The drawings filed on *27 November 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 12/1/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20050525*.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. Claims 16-44 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statement filed December 1, 2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because it was not submitted with either a statement under 37 CFR 1.97(e) or the $240 fee under 37 CFR 1.17(p) as required under 37 CFR 1.97(c). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael G. Verga on May 25, 2005.

The application has been amended as follows wherein the following listings of claims 16-20, 22-28, 30, 32-38, and 40-44 replace all prior listings in their entirety:

16. A source synchronous link comprising:

a communication link;

a source synchronous transmitter constructed and arranged to transmit a data signal and ~~at least one~~ a differential data strobe signal over said communication link, wherein said source synchronous transmitter is configured to halt said ~~at least one~~ differential data strobe signal in a selected one of two alternative logical states in response to an external condition; and

a source synchronous receiver, coupled to said communication link, that clocks in said data signal in accordance with said ~~at least one~~ differential data strobe signal, wherein when said ~~at least one~~ differential data strobe signal is halted, said data signal is not clocked into said source synchronous receiver.

17. The source synchronous link of claim 16, wherein said source synchronous receiver comprises data capture flip-flops controlled by said ~~one or more~~ differential data strobe signal~~s~~, wherein when said ~~at least one~~ differential data strobe signal is halted, subsequently-received data signals are not written to said data capture flip-flops.

18. The source synchronous link of claim 16, wherein said source synchronous transmitter comprises:

data strobe transmit logic configured to transmit said ~~at least one~~ differential data strobe signal over at least one clock line of said communication link, and to maintain said ~~at least one~~ differential data strobe signal in a the selected one of two alternative logical state~~s~~ in response to said external condition halting said differential data strobe signal.

20. The source synchronous link of claim 18, wherein said ~~at least one~~ differential data

strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

22. The source synchronous link of claim 20, wherein said data strobe transmit logic comprises:

a differential data strobe signal generator configured to select from a first two available signals to generate said first data strobe signal and to select from a second two available signals to generate said second data strobe signal; and

strobe stopping logic that controls logic levels of said first two available signals and said second two available signals, wherein to halt said ~~at least one~~ differential data strobe signal said strobe stopping logic sets said first two available signals to a same first logic level and sets said second two available signals to a same second logic level different than said same first ~~same~~ logic level.

23. The source synchronous link of claim 16, wherein said ~~at least one~~ differential data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

24. The source synchronous link of claim 23, wherein said first data strobe signal and said second data strobe signal may be transmitted at either one of two logical states and wherein said data strobe transmit logic maintains said first data strobe signal at a first of said two logical states and maintains said second data strobe signal at a second of said two logical states when said data strobe transmit logic halts said ~~one or more~~ differential data strobe signals.

25. The source synchronous link of claim ~~16~~ 23,

wherein when operating in a normal mode of operation said source synchronous transmitter toggles said first data strobe signal between two logical states, and toggles said second data strobe signal between the two logical states, and

wherein when operating in a data capture debug mode of operation, said source synchronous transmitter halts said first data strobe signal at one of said two logical states, and halts said second data strobe signal at the other one of said two logical states.

26. A circuit comprising:

a communication link;

a first processing core comprising a source synchronous transmitter constructed and arranged to transmit a data signal and ~~at least one~~ a differential data strobe signal over said communication link, wherein said transmitter is configured to halt said ~~at least one~~ differential data strobe signal in a selected one of two alternative logical states in response to an external condition; and

a second processing core comprising a source synchronous receiver, coupled to said communication link, that clocks in said data signal in accordance with said ~~at least one~~ differential data strobe signal, wherein when said ~~at least one~~ differential data strobe signal is halted, said data signal is not clocked into said source synchronous receiver.

27. The circuit of claim 26, wherein said source synchronous receiver comprises data capture flip-flops controlled by said ~~one or more~~ differential data strobe signal~~s~~, wherein when said ~~at least one~~ differential data strobe signal is halted, subsequently-received data signals are not written to said data capture flip-flops.

28. The circuit of claim 26, wherein said source synchronous transmitter comprises:

data strobe transmit logic configured to transmit said ~~at least one~~ differential data strobe signal over at least one clock line of said communication link, and to maintain said ~~at least one~~ differential data strobe signal in a the selected one of two alternative logical states in response to said external condition halting said differential data strobe signal.

30. The circuit of claim 28, wherein said ~~at least one~~ differential data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

32. The circuit of claim 30, wherein said data strobe transmit logic comprises:

a differential data strobe signal generator configured to select from a first two available signals to generate said first data strobe signal and to select from a second two available signals to generate said second data strobe signal; and

strobe stopping logic that controls logic levels of said first two available signals and said second two available signals, wherein to halt said ~~at least one~~ differential data strobe signal said strobe stopping logic sets said first two available signals to a same first logic level and sets said second two available signals to a same second logic level different than said same first ~~same~~ logic level.

33. The circuit of claim 26, wherein said ~~at least one~~ differential data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

34. The circuit of claim 33, wherein said first data strobe signal and said second data strobe signal may be transmitted at one of either two logical states, and wherein said data strobe transmit logic maintains said first data strobe signal at a first of said two logical states and maintains said second data strobe signal at a second of said two logical states when said data strobe transmit logic halts said ~~one or more~~ differential data strobe signal~~s~~.

35. A source synchronous link comprising:

a communication link;

transmitting means, coupled to said communication link, for transmitting a data signal and ~~at least one~~ a differential data strobe signal over said communication link, wherein said transmitter is configured to halt said ~~at least one~~ differential data strobe signal in a selected one of two alternative logical state~~s~~ in response to an external condition; and

receiving means, coupled to said communication link, for clocking in said data signal in accordance with said ~~at least one~~ differential data strobe signal, wherein when said ~~at least one~~ differential data strobe signal is halted, said data signal is not clocked into said ~~source synchronous receiver~~ receiving means.

36. The source synchronous link of claim 35, wherein said receiving means comprises:

data capture flip-flops controlled by said ~~one or more~~ differential data strobe signals,

wherein when said ~~one or more~~ differential data strobe signals are halted, subsequently-received data signals are not written to said data capture flip-flops.

37. The source synchronous link of claim 35, wherein said transmitting means comprises:

data strobe transmitting means for transmitting said ~~at least one~~ differential data strobe signal over at least one clock line of said communication link that corresponds to said data line, and for maintaining said ~~at least one~~ differential data strobe signal in a selected logical state in response to said external condition halting said differential data strobe signal.

38. The source synchronous link of claim 37, wherein said ~~at least one~~ differential data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

40. The source synchronous link of claim 38, wherein said data strobe transmitting means comprises:

differential data strobe signal generating means for selecting from a first two available signals to generate said first data strobe signal and for selecting from a second two available signals to generate said second data strobe signal; and

strobe stopping means for controlling logic levels of said first two available signals and said second two available signals, wherein to halt said ~~at least one~~ differential data strobe signal said strobe stopping means sets said first two available signals to a same first logic level and sets said second two available signals to a same second logic level different than said ~~first same~~ same first logic level.

41. A method for transmitting data and corresponding data strobes over a source synchronous link having a communication link coupling a transmitter and a receiver, comprising:

transmitting a data signal and ~~at least one~~ a differential data strobe signal over said communication link;

halting said ~~at least one~~ differential data strobe signal in a selected one of two alternative logical states in response to an external condition; and

receiving into said receiver said data signal in accordance with said ~~at least one~~ differential data strobe signal unless said ~~at least one~~ differential data strobe signal is halted.

42. The method of claim 41, wherein said receiver comprises data capture flip-flops, and wherein the method further comprises:

clocking said data signal into said data capture flip-flops in accordance with said ~~one or more~~ differential data strobe signals;

ceasing to clock said data signal into said data capture flip-flops when said ~~one or more~~ differential data strobe signal~~s are~~ is halted.

43. The method of claim 41, wherein transmitting ~~at least one~~ said differential data strobe signal comprises:

transmitting a first data strobe signal; and

transmitting a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

44. The method of claim 43, wherein ~~transmitting at least one data strobe signal comprises~~:

transmitting a first data strobe signal comprises selecting from a first two available signals to generate said first data strobe signal;

transmitting a second data strobe signal comprises selecting from a second two available signals to generate said second data strobe signal;

controlling logic levels of said first two available signals and said second two available signals; and

setting said first two available signals to a same first logic level and setting said second two available signals to a same second logic level different than said same first ~~same~~ logic level to halt said ~~at least one~~ differential data strobe signal.

Claims 16-44 are renumbered respectively as claims 1-28, and the claim dependency is renumbered accordingly.

Allowable Subject Matter

4. Claims 16-44 renumbered respectively as claims 1-28 are allowed.

5. The following is an examiner's statement of reasons for allowance:

Claims 16-44 renumbered respectively as claims 1-28 are allowed over the prior art of record because the prior art of record does not disclose or obviate the halting of a differential data strobe in a selected one of two alternative states to thereby prevent the clocking of a transmitted data signal over a communications link. While the prior art of record, namely Keeth et al (US 6026051), discloses halting a differential data strobe signal as applied in the art rejections of the previous office actions, it does not disclose that the halted data strobe may be halted in a specified one of two alternative states as

claimed. Rather, if the differential data strobe of Keeth et al is halted via the enable signal (fig. 3, ref. enable*), the differential data strobe signals DCLK0OUT and DCLK0OUT* are halted at the respective levels of VCC and GND and may not take on any alternative logic state.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
May 25, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER